ABSTRACT

A three-dimensional ("3-D") memory capacitor comprises a bottom electrode, a ferroelectric thin film, and a top electrode that conform to a 3-D surface of an insulator layer. The capacitance area is greater than the horizontal footprint area of the capacitor. Preferably, the footprint of the capacitor is less than 0.2 nm^2, and the corresponding capacitance area is typically in a range of from 0.4 nm^2 to 1.0 nm^2 The ferroelectric thin film preferably has a thickness not exceeding 60 nm. A capacitor laminate including the bottom electrode, ferroelectric thin film, and the top electrode preferably has a thickness not exceeding 200 nm. A low-thermal-budget MOCVD method for depositing a ferroelectric thin film having a thickness in a range of from 30 nm to 90 nm includes an RTP treatment before depositing the top electrode and an RTP treatment after depositing the top electrode and etching the ferroelectric layer.